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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,383	08/31/2001	Arulkumar P. Shanmugasundram	5920/FET/DV	7797

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EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 02/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,383	SHANMUGASUNDRAM ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-76* is/are pending in the application.

4a) Of the above claim(s) *55-72* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-54 and 73-76* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-54 and 73-76 are rejected under 35 U.S.C. 102(e) as being anticipated by Pasadyn et al., U.S. Patent 6,588,007 B1.

Pasadyn discloses a semiconductor process as claimed. See **FIGS. 1-5** where Pasadyn teaches the claimed invention.

3. Pertaining to claim 1, Pasadyn teaches a method for controlling one or more wafer properties in a semiconductor processing tool using data collected from an in situ sensor, where at least one of said one or more wafer properties comprises within-wafer uniformity, said method comprising the steps of:

(1) setting recipe parameters relating to said wafer property according to a process model, wherein said model is used to predict wafer outputs **(FIG. 4)**;

(2) executing a process on a wafer with the tool according to said recipe parameters;

(3) collecting data (see **FIG. 4**) relating to said one or more wafer properties during execution of said process with said in situ sensor;

(4) adjusting said process by modifying said recipe parameters according to comparisons between said data collected by said in situ sensor relating to said wafer properties and results predicted by said model; and

(5) using said data collected by said in situ sensor in a process on a subsequent wafer to be executed by the tool (see **FIG. 9** also this is well known as a run-to-run process).

4. Pertaining to claim 2, Pasadyn teaches the method of claim 1, wherein said property comprises wafer thickness due to a CMP (chemical-mechanical polish process the thickness of the wafer will change).

5. Pertaining to claim 3, Pasadyn teaches the method of claim 1, wherein said tool comprises a polishing device.

6. Pertaining to claim 4, Pasadyn teaches the method of claim 1, wherein said tool comprises a plurality of processing resources, each of which includes an in situ sensor, and wherein data from one in situ sensor may be forwarded to another processing resource in real time during execution of said process.

7. Pertaining to claim 5, Pasadyn teaches the method of claim 1, further comprising the step of collecting data from an inline sensor; and

integrating said data collected from said inline sensor with said data collected from said in situ sensor before processing said subsequent wafer (hence, run-to-run process).

8. Pertaining to claim 6, Pasadyn teaches the method of claim 5, wherein data collected from said inline sensor is utilized to calibrate said in situ sensor.

9. Pertaining to claim 7, Pasadyn teaches the method of claim 1, further comprising the step of collecting data from a sensor located at an upstream tool; and

integrating said data collected from said upstream tool with said data collected from said in situ sensor before processing said subsequent wafer.

10. Pertaining to claim 8, Pasadyn teaches the method of claim 7, wherein data collected from said upstream tool is utilized to calibrate said in situ sensor.

11. Pertaining to claim 9, Pasadyn teaches the method of claim 1, wherein said parameters include a processing time (column 11, line 58).

12. Pertaining to claim 10, Pasadyn teaches the method of claim 1, wherein said data collected by said in situ sensor is used for run- to-run control on subsequent wafers processed by said tool.

13. Pertaining to claim 11, Pasadyn teaches the method of claim 1, wherein said tool comprises a plurality of processing devices, each of which includes an in situ sensor, and wherein data from one in situ sensor may be compared with data from another in situ sensor to in real time to compare results from each device.

14. Pertaining to claim 12, Pasadyn teaches a method for controlling a one or more wafer properties in a semiconductor processing tool using data collected from an in situ sensor, where at least one of said one or more wafer properties comprises within-wafer uniformity, said method comprising the steps of:

(1) collecting data with said in situ sensor relating to said one or more wafer properties during a process executed according to wafer recipe parameters;

(2) adjusting said process by modifying said recipe parameters according to comparisons between said data collected by said in situ sensor relating to said wafer properties and results predicted by a process model used to predict wafer outputs; and

(3) using said data collected by said in situ sensor in a process on a subsequent wafer to be executed by the tool.

15. Pertaining to claim 13, Pasadyn teaches the method of claim 12, wherein said step of adjusting comprises increasing or decreasing a processing time.

16. Pertaining to claim 14, Pasadyn teaches the method of claim 13, wherein said processing time comprises polishing time.

17. Pertaining to claim 15, Pasadyn teaches the method of claim 12, wherein said tool comprises a plurality of processing resources, each of which includes an in situ sensor, and wherein data from one in situ sensor may be forwarded to another processing resource in real time during execution of said process.

18. Pertaining to claim 16, Pasadyn teaches the method of claim 12, further comprising the step of collecting data from an inline sensor; and

integrating said data collected from said inline sensor with said data collected from said in situ sensor before processing said subsequent wafer.

19. Pertaining to claim 17, Pasadyn teaches the method of claim 12, further comprising the step of collecting data from a sensor located at an upstream tool; and

integrating said data collected from said upstream tool with said data collected from said in situ sensor before processing said subsequent wafer.

20. Pertaining to claim 18, Pasadyn teaches the method of claim 12, wherein said data collected by said in situ sensor is used for run-to-run control on subsequent wafers processed by said tool.

21. Pertaining to claim 19, Pasadyn teaches a system for controlling one or more wafer properties, where at least one of said one or more wafer properties comprises within-wafer uniformity, comprising:

a semiconductor processing tool capable of executing a process for processing a wafer according to recipe parameters relating to one or more wafer properties;

an in situ sensor configured to collect data relating to said one or more wafer properties during execution of said process; and

a processor useable for setting said recipe parameters according to a process model for predicting wafer outputs, wherein said processor is utilizable for adjusting said process by modifying said recipe parameters according to comparisons between said data collected by said in situ sensor relating to said one or more wafer properties and results predicted by said model, and wherein said processor uses said data collected by said in situ sensor in a process on a subsequent wafer to be executed by the tool.

22. Pertaining to claim 20, Pasadyn teaches the system of claim 19, wherein said on or more wafer properties comprises wafer thickness.

23. Pertaining to claim 21, Pasadyn teaches the system of claim 19, wherein said tool comprises a polishing device.

24. Pertaining to claim 22, Pasadyn teaches the system of claim 19, wherein said tool comprises a plurality of processing resources, each of which includes an in situ sensor, and

wherein data from one in situ sensor may be forwarded to another processing resource in real time during execution of said process.

25. Pertaining to claim 23, Pasadyn teaches the system of claim 19, further comprising an inline sensor configured to collect data, wherein said data collected from said inline sensor is integrated with said data collected from said in situ sensor before processing said subsequent wafer.

26. Pertaining to claim 24, Pasadyn teaches the system of claim 23, wherein data collected from said inline sensor is utilized to calibrate said in situ sensor.

27. Pertaining to claim 25, Pasadyn teaches the system of claim 19, further comprising a sensor located at an upstream tool configured to collect data, wherein said data collected from said upstream tool is integrated with said data collected from said in situ sensor before processing said subsequent wafer.

28. Pertaining to claim 26, Pasadyn teaches the system of claim 25, wherein data collected from said upstream tool is utilized to calibrate said in situ sensor.

29. Pertaining to claim 27, Pasadyn teaches the system of claim 19, wherein said parameters include a processing time.

30. Pertaining to claim 28, Pasadyn teaches the system of claim 19, wherein said data collected by said in situ sensor is used for run-to-run control on subsequent wafers processed by said tool.

31. Pertaining to claim 29, Pasadyn teaches the system of claim 19, wherein said tool comprises a plurality of processing devices, each of which includes an in situ sensor, and

wherein data from one in situ sensor may be compared with data from another in situ sensor to in real time to compare results from each device.

32. Pertaining to claim 30, Pasadyn teaches a system for controlling one or more wafer properties, where at least one of said one or more wafer properties comprises within-wafer uniformity comprising:

an in situ sensor for collecting data relating to said on or more wafer properties during a process executed by a semiconductor processing tool according to wafer recipe parameters;

a processor configured to adjust said process by modifying said recipe parameters according to comparisons between said data collected by said in situ sensor relating to said one or more wafer properties and results predicted by a process model used to predict wafer outputs; and

wherein said processor is configured to use said data collected by said in situ sensor in a process on a subsequent wafer to be executed by the tool.

33. Pertaining to claim 31, Pasadyn teaches the system of claim 30, wherein said processor is configured to increase or decrease a processing time of the tool.

34. Pertaining to claim 32, Pasadyn teaches the system of claim 31, wherein said processing time comprises polishing time.

35. Pertaining to claim 33, Pasadyn teaches the system of claim 30, wherein said tool comprises a plurality of processing resources, each of which includes an in situ sensor, and wherein data from one in situ sensor may be forwarded to another processing resource in real time during execution of said process.

36. Pertaining to claim 34, Pasadyn teaches the system of claim 30, further comprising an inline sensor configured to collect data, and wherein said inline sensor is adapted to integrate

said collected data with said data collected from said in situ sensor before processing said subsequent wafer.

37. Pertaining to claim 35, Pasadyn teaches the system of claim 30, further comprising a sensor located at an upstream tool configured to collect data, and wherein said sensor is adapted to integrate said collected data with said data collected from said in situ sensor before processing said subsequent wafer.

38. Pertaining to claim 36, Pasadyn teaches the system of claim 30, wherein said data collected by said in situ sensor is used for run-to-run control on subsequent wafers processed by said tool.

39. Pertaining to claim 37, Pasadyn teaches a system for controlling one or more wafer properties in a semiconductor processing tool using data collected from an in situ sensor,where at least one of said one or more wafer properties comprises within-wafer uniformity, said system comprising:

means for setting recipe parameters relating to said one or more wafer properties according to a process model, wherein said model is used to predict wafer outputs;

means for executing a process on a wafer with the tool according to said recipe parameters;

means for collecting data relating to said one or more wafer properties during execution of said process with said in situ sensor;

means for adjusting said process by modifying said recipe parameters according to comparisons between said data collected by said in situ sensor relating to said wafer property and results predicted by said model; and

means for using use said data collected by said in situ sensor in a process on a subsequent wafer to be executed by the tool.

40. Pertaining to claim 38, Pasadyn teaches the system of claim 37, wherein said one or more wafer properties comprises wafer thickness.

41. Pertaining to claim 39, Pasadyn teaches the system of claim 37, wherein said tool comprises a polishing device.

42. Pertaining to claim 40, Pasadyn teaches the system of claim 37, wherein said tool comprises a plurality of processing resources, each of which includes an in situ sensor, and wherein data from one in situ sensor may be forwarded to another processing resource in real time during execution of said process.

43. Pertaining to claim 41, Pasadyn teaches the system of claim 37, further comprising means for collecting data from an inline sensor; and

means for integrating said data collected from said inline sensor with said data collected from said in situ sensor before processing said subsequent wafer.

44. Pertaining to claim 42, Pasadyn teaches the system of claim 41, wherein data collected from said inline sensor is utilized to calibrate said in situ sensor.

45. Pertaining to claim 43, Pasadyn teaches the system of claim 37, further comprising means for collecting data from a sensor located at an upstream tool; and

means for integrating said data collected from said upstream tool with said data collected from said in situ sensor before processing said subsequent wafer.

46. Pertaining to claim 44, Pasadyn teaches the system of claim 43, wherein data collected from said upstream tool is utilized to calibrate said in situ sensor.

47. Pertaining to claim 45, Pasadyn teaches the system of claim 37, wherein said parameters include a processing time.

48. Pertaining to claim 46, Pasadyn teaches the system of claim 37, wherein said data collected by said in situ sensor is used for run-to-run control on subsequent wafers processed by said tool.

49. Pertaining to claim 47, Pasadyn teaches the system of claim 37, wherein said tool comprises a plurality of processing devices, each of which includes an in situ sensor, and wherein data from one in situ sensor may be compared with data from another in situ sensor to in real time to compare results from each device.

50. Pertaining to claim 48, Pasadyn teaches a system for controlling one or more wafer properties in a semiconductor processing tool using data collected from an in situ sensor, where at least one or more wafer properties comprises within-wafer uniformity, said system comprising:

means for collecting data with said in situ sensor relating to said one or more wafer properties during a process executed according to wafer recipe parameters;

means for adjusting said process by modifying said recipe parameters according to comparisons between said data collected by said in situ sensor relating to said one or more wafer properties and results predicted by a process model used to predict wafer outputs; and

means for using said data collected by said in situ sensor in a process on a subsequent wafer to be executed by the tool.

51. Pertaining to claim 49, Pasadyn teaches the system of claim 48, wherein said means for adjusting comprises means for increasing or decreasing a processing time.

52. Pertaining to claim 50, Pasadyn teaches the system of claim 49, wherein said processing time comprises polishing time.

53. Pertaining to claim 51, Pasadyn teaches the system of claim 48, wherein said tool comprises a plurality of processing resources, each of which includes an in situ sensor, and wherein data from one in situ sensor may be forwarded to another processing resource in real time during execution of said process.

54. Pertaining to claim 52, Pasadyn teaches the system of claim 48, further comprising means for collecting data from an inline sensor; and

means for integrating said data collected from said inline sensor with said data collected from said in situ sensor before processing said subsequent wafer.

55. Pertaining to claim 53, Pasadyn teaches the system of claim 48, further comprising means for collecting data from a sensor located at an upstream tool; and

means for integrating said data collected from said upstream tool with said data collected from said in situ sensor before processing said subsequent wafer.

56. Pertaining to claim 54, Pasadyn teaches the system of claim 48, wherein said data collected by said in situ sensor is used for run-to-run control on subsequent wafers processed by said tool.

57. Pertaining to claim 73, Pasadyn teaches a method for controlling within-wafer uniformity in a semiconductor processing tool using data collected from an in situ sensor, said method comprising the steps of:

(1) setting recipe parameters relating to said within-wafer uniformity according to a process model, wherein said model is used to predict wafer outputs;

(2) executing a process on a wafer with the tool according to said recipe parameters;

(3) collecting data relating to said within-wafer uniformity during execution of said process with said in situ sensor;

(4) adjusting said process by modifying said recipe parameters according to comparisons between said data collected by said in situ sensor relating to said within-wafer uniformity and results predicted by said model.

58. Pertaining to claim 74, Pasadyn teaches the method of claim 73, wherein said tool comprises a polishing device.

59. Pertaining to claim 75, Pasadyn teaches the method of claim 73, further comprising the step of comprises a plurality of processing resources, each of which includes an in situ sensor, and wherein data from one in situ sensor may be forwarded to another processing resource in real time during execution of said process.

60. Pertaining to claim 76, Pasadyn teaches the method of claim 73, further comprising the step of collecting data from an inline sensor; and

Integrating said data collected from said inline sensor with said data collected from said in situ sensor before processing said subsequent wafer.

Conclusion

61. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

62. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

63. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on 9:00 AM-5:00 PM.

64. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

65. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. David Coleman
Primary Examiner
Art Unit 2823

WDC